UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

17

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,717	10/31/2003	Krzysztof Nauka	5649-2234	1558

20792 7590 09/05/2007

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
PHAM, VAN T	

ART UNIT	PAPER NUMBER
2627	

MAIL DATE	DELIVERY MODE
09/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,717	NAUKA ET AL.	
	Examiner	Art Unit	
	VAN T. PHAM	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7,9,11 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7, 9, 11 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. The Appeal Brief filed on 5/20/2007 is noted. In view of the arguments therein and the newly discovered reference(s) to Yano et al. (US 5,985,404), and Cho et al. (US 2004/0090903), rejections based on the newly cited reference(s) follow.

2. Applicant's arguments with respect to claims 7, 11 and 28 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 5/20/2007 have been fully considered but they are not persuasive.

Claim 9:

First of all, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Kasanuki doesn't teach or suggest block erasure by dragging a probe tip, nor does Kasanuki disclose erasing **multiple bits at a time**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

However, Applicant pointed out that paragraph 30 states that a block erasure can be performed "by dragging the probe tip along the ferroelectric layer across multiple bits at the time", noted that in the specification state that

> "*A bit 413* can be locally erased by bringing the probe tip into position where the bit 413 was previously written and then having the circuit 120 apply reverse bias to the probe 112, so the local polarization is brought to the polarization of the surrounding ferroelectric medium. A *block erasure can be performed by dragging the probe tip along the ferroelectric layer 118 across multiple bits 413*".

Which does not mean that "dragging the probe tip along the ferroelectric layer across multiple bits ***at the time*** ".

Second of all, Kasanuki does disclose or suggest block erasure by dragging a probe tip,

see Kasanuki, col. 4, lines 47-61, discloses

"In an information processing apparatus using a recording medium based on the principles of an STM and formed from a ferroelectric substance, information is written by applying an electric field based on the principles of an STM. Reading of information is performed by a complicated method in which a recording layer is heated by laser beam irradiation or high-frequency heating, the recording medium is activated pyroelectrically, and signals which occur are detected by an ultra-high resolution electrometer probe in a standard electrometer. It cannot be said that this is a simple method. The information processing apparatus shown in FIG. 13 has a problem in that when **a probe or a recording medium is scanned two-dimensionally in X and Y directions,** resonance is likely to occur in the scanning mechanism if the scanning frequency increases".

Moreover, col. 3, lines 1-15 of Kasanuki discloses

"To perform recording, an application of a pulse voltage greater than a threshold voltage causes electric charge from the silicon substrate 111 to tunnel through the SiO.sub.2 film 112 and to be trapped in an SiN film 113. As a result, information is recorded. To perform reproducing, an appropriate bias is applied to the recording medium and the probe electrode 1, a modulation signal is carried thereon, and capacitance changes during the scanning of the probe electrode 1 are detected. Since the capacitance between the probe electrode 1 and the recording medium changes depending upon whether a charge is trapped in the SiN film 113, information can be read out. **To perform erasing, it is only necessary to apply a pulse voltage of the polarity opposite to that during recording.**"

Therefore, by having the probe is scanned two-dimensionally in X and Y directions to perform erasing by apply a pulse voltage of the polarity opposite to that during recording, which is performing the probe perform block and erasure operation". Also, Applicant agreed that "Kasanuki's devices perform erasure the same way that information is recorded: one bit at a time (see Kasanuki col. 12, lines 52-56 and col. 18, lies 14-2)". Clearly, Kanasuki discloses that a circuit for causing the probe 1 to perform block and bulk erasure operations.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Kasanuki et al. (US 5,481,527).

Regarding claim 9, Kasanuki discloses a data storage device comprising a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1 and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col. 8, line 21); and a circuit for causing the conductive probe to perform block and bulk erasure operations (see response).

5. Claims 11 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho et al. (US 2004/0090903).

Regarding claim 11, Cho et al. discloses a data storage device comprising

a conductive probe having a tip (see Fig. 1, element 11);

a substrate including a semiconductor portion (see Fig. 1, elements 15-16 and [0060]);

a data storage medium including a layer of poled ferroelectric material for storing data, the ferroelectric layer on the substrate, between the tip and the substrate, the semiconductor

portion and the ferroelectric layer forming an electrical junction (see Fig. 1, tip 11, ferroelectric layer 17, semiconductor layer 15, electrode layer 16, and see); and

a read circuit for using the probe to sense changes in capacitance or leakage current of the junction (see abstract and Fig. 1, [0008]).

Regarding claim 28, a method of reading information from a ferroelectric layer that is on a semiconductor substrate, and forms an electrical junction with the semiconductor substrate, the method comprising:

scanning a surface of the ferroelectric layer with a probe having a sharp tip, the tip having a diameter of several nanometers (see Fig. 1 and [0050]); and

using the probe and the semiconductor substrate to detect polarity reversals at designated locations on the ferroelectric layer (Fig. 3), each polarity reversal at a designated location indicating a first stored value at that designated location, each non-reversal of polarity at an expected location indicating a second logic value stored at that designated location (see [0061]);

wherein the probe is used to sense changes in capacitance or leakage current of the junction (see Fig. 1, [0072], [0075]-[0077]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being anticipated by Kasanuki et al. (US 5,481,527) in view of Yano et al. (Us 5,985,404).

Regarding claim 7, Kasanuki discloses a data storage device comprising: a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1 and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col.8, line 21).

Yano et al. (Us 5,985,404) discloses a protective layer having a relatively high hardness prevents the ferroelectric layer on its surface from mechanical damages by collision of the probe or the like. Moreover, the protective layer is given appropriate conductivity, the electric charge on the ferroelectric layer surface is made uniform, preventing the concentration of electric charge from locally occurring on the ferroelectric layer surface by the pyroelectric effect and crystal deflects of the ferroelectric and accordingly, preventing noise and probe failure by the concentrated electric charge (see Yano col. 6, lines 16-37 and Fig. 5, col. 21, lines 58-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a protective layer in Kasanuki as suggested by Yano, the motivation being in order for preventing noise and probe failure by the concentrated electric charge (see Yano col. 6, lines 16-37 and Fig. 5, col. 21, lines 58-65).

Cited References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The cited references relate to dielectric recording apparatus dielectric reproducing apparatus.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN T. PHAM whose telephone number is 571-272-7590. The examiner can normally be reached on Monday-Thursday from 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VP

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER